REMARKS

In light of the Examiner's new grounds for rejection, Applicants have further modified the claims to additionally specify that there is substantially none of the protective material formed on the side of the chip at which the electrodes are located. Furthermore, the claims have been modified to specify that each of the side surfaces for each individual chip has the protective resin applied thereto.

Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicants presently claimed invention as now specified. More specifically, Applicants note that the Farnworth reference, United States patent number 5,933,713 actually teaches away from Applicants presently claimed structure in that it explicitly teaches that an encapsulant envelope 60 which is comprised of the encapsulant material layers 42 and 50 completely surrounds an individual semiconductor chip member and specifically includes encapsulant layer 42 overlying the active surface 22, the surface of the prior art chip at which the electrodes are located.

This is substantially different than Applicants presently claimed invention wherein the resin material is applied to the semiconductor chips during the manufacturing process when the chips have their respective electrode surfaces secured to an adhesive layer. As a result, substantially none of the protective resin material is applied to the surface of the chips at which the electrodes are located. In accordance with the prior art Farnworth patent, solder paste 28 is reflowed to form substantially spherical balls 30 which are subsequently planarized. Thereafter a molten encapsulating material is injected under pressure to form a

layer of encapsulant 42 over the active surface 22. It should be apparent that Farnsworth is directed to a much different semiconductor chip processing technique and therefore neither teaches nor suggest Applicants presently claimed invention. As noted above, this reference actually teaches away from the claimed invention as now specified wherein no resin is applied to the surface of the chips at which the electrodes are located. See specifically column 7 at lines 6-42 and column 9 at lines 25-32

Applicants also submit that the remaining references of record similarly failed to teach or suggest applicants presently claimed invention. More specifically, Applicants note that the Paik prior art reference, United States patent number 5,879,964 is directed to a substantially different manufacturing technique wherein during a two-stage process a plurality of wafers strips 2 each including several dies or individual chip members are cut and secured to a polyimide film and a polymer dam 6 made of an epoxy based polymer exhibiting high viscosity is formed on the surface of the film to which the wafers strips are bonded.

An epoxy based polymer exhibiting low viscosity is then filled in the wafer region defined by the polymer 6, thereby forming an encapsulant 7 which encapsulates the wafer strips. This process does not provide any of the resin at adjacent side surfaces of the wafers strips which include a plurality of chips that can have not been separated. More specifically, not all of the individual chips have resin located at side surfaces thereof in accordance with the manufacturing technique described in this prior art reference. Accordingly this is one distinction between the prior art and presently claimed invention.

Yet another distinction relating to this prior art reference is that the wafer structure is encapsulated completely and via holes 8 eight are necessarily formed at positions respectively corresponding to pads of the chips through the film 4 remaining on the wafer structure. See specifically column 4 at lines 15-45. Accordingly, it is also apparent that this prior art reference similarly relates to a much different manufacturing technique which actually teaches away from the subject matter now specified in the instant claims.

In light of the foregoing, Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest the presently claimed invention. Accordingly, Applicants respectfully request that the Examiner now withdraw all rejections and allow all of the claims.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-1794.

Respectfully submitted,

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(Reg. #37,607)

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